| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/668,974 | SHIMIZU ET AL. | |
| | Examiner | Art Unit | |
| | Mary C. Jacob | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments filed 10/20/06*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20061226* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

1. Claims 1-12 have been presented for examination.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ronald Coslick (Reg. 36,489) on 12/21/06.

3. The application has been amended as follows:

Claim 1 has been replaced with

--1. A circuit simulation apparatus comprising:

a simulation executing unit which reads a circuit net list in which connection descriptions of a circuit to be simulated are stored, and which calculates changes in the current and voltage of said circuit to be simulated, using a transistor model, and

a diffusion-length-dependent parameter correcting unit which creates an approximate expression for determining a corrected value of a diffusion-length-dependent parameter for a transistor model created for a transistor having a predetermined diffusion length, and which calculates and stores a corrected

value of said diffusion-length-dependent parameter for said transistor model used by the simulation executing unit using said approximate expression to model a transistor having a diffusion length different from that of said transistor model, wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and wherein said diffusion length of said transistor is defined by a distance between boundaries of said isolation region in a direction from the source region to the drain region. --

Claim 2, line 2, the phrase "parameter includes" was changed to -- parameters include--.

Claim 3, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 4, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 5, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 6, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 7 has been replaced with

--7. A transistor model creating method comprising the steps of:

creating a transistor model on the basis of the characteristics of a MOS transistor having a predetermined diffusion length,

extracting diffusion-length-dependent parameters for each of a plurality of MOS transistors having diffusion lengths different from said predetermined diffusion length,

creating approximate expressions representing a diffusion length dependence of said diffusion-length-dependent parameters for said plurality of MOS transistors,

calculating corrected values of said diffusion-length-dependent parameters for a transistor having a diffusion length different than said predetermined diffusion length, using one or more of said approximate expressions,

and

creating and storing a corrected transistor model using said corrected values of said diffusion-length-dependent parameters,

wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and

wherein said diffusion length of said transistor is defined by a distance between boundaries of said isolation region in a direction from the source region to the drain region.--

Claim 8, the phrase "parameter includes" was changed to --parameters include--.

Claim 9, line 2, the phrase "the corrected approximate" was changed to --the approximate--.

Claim 10, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 11, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

Claim 12, line 2, the phrase "the corrected approximate" was changed to -- the approximate--.

***Specification***

4. The amendments to the specification are withdrawn due to the Amendment filed 10/20/06.

***Claim Objections***

5. The objections to the claims are withdrawn due to the Amendment filed 10/20/06.

***Claim Rejections - 35 USC § 112***

6. The objections under 35 U.S.C. 112, second paragraph, are withdrawn due to the Amendment filed 10/20/06 and the Examiner's Amendment above.

***Allowable Subject Matter***

7. Claims 1-12 are allowed.

8. The following is an examiner's statement of reasons for allowance:

While Chu et al ("A Database-Driven VLSI Design System", IEEE Transactions on Computer-Aided Design, Vol, CAD-5, No. 1, January 1986) teaches a VLSI database design system that stores information about a transistor parameters including their corresponding diffusion size, Chung et al ("An Analytical Threshold-Voltage Model of Trench-Isolated MOS Devices with Nonuniformly Doped Substrates", IEEE Transactions on Electron Devices, Vol. 39, No. 3, March 1992) teaches determining an expression of the threshold voltage for a Trench-Isolated MOS device that includes adding a correction factor and creating a corrected approximate expression for the threshold voltage and further creating and simulating a corrected transistor model, and Zhang et al (US Patent 6,618,837) teaches a parameter correcting unit which creates corrected parameters for a transistor model, none of these references taken either alone or in combination with the prior art of record disclose a diffusion-length-dependent parameter correcting unit which creates an approximate expression for determining a corrected value of a diffusion-length-dependent parameter for a transistor, specifically including:

(claims 1 and 7) "wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and

wherein said diffusion length of said transistor is defined by a distance between boundaries of said isolation region in a direction from the source region to the drain region"

in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Aggarwal et al ("A Methodology for Pre-Determination of Bipolar SPICE Model Parameters in BICMOS Technology", Proceedings of IEEE International Conference on Microelectronic Test Structures, Vol. 6, March 1993) teaches obtaining SPICE model parameters for bipolar devices of varying sizes available in BiCMOS technology including the lateral diffusion (size variation).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
12/26/06

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
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12/29/06